# Pattern Generator Module

## L-6001-EPG428-1

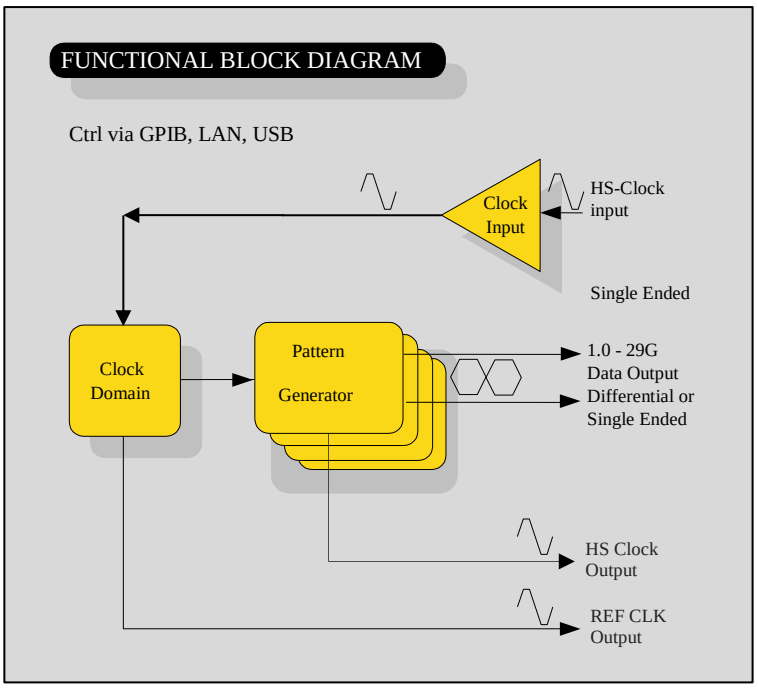
### DESCRIPTION

EPG428 is an Electrical Pattern Generator module that plugs into the PARALLEX® Chassis. EPG428 can generate 4 channel electrical data from 1 Gb/s up to 29 Gb/s continuously. A half-rate input clock is required and it can be daisy-chained to the Error detector and additional modules. Therefore it is an ideal solution for 100Gb/s and future 400Gb/s applications.


PATTERN GENERATOR MODULE PN: L-6001-EP428-1

### KEY FEATURES

- Data Rates 1 to 29 Gbps
- 4 channels
- Operates with half rate clock
- Differential Electrical Pattern Generator (K Connector)
- Reference clock output to drive SERDES, CDR that require low speed clock
- PRBS pattern: 9, 15, 31
- Data output polarity swap
- High speed Clock Input and Output
- GPIB/LAN/USB Interface via PARALLEX® Chassis.
- Small size: width 50.8mm (2”)




EPG428

Product Brief

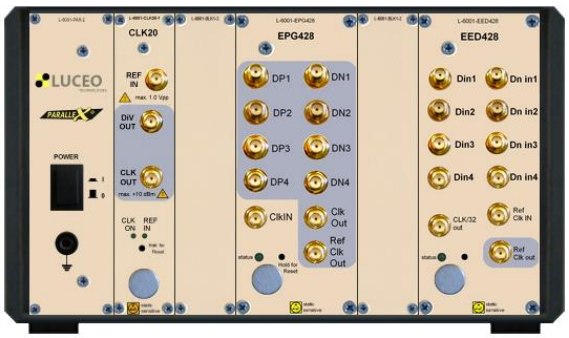
# Pattern Generator Module L-6001-EPG428-1

## KEY PERFORMANCE PARAMETERS

| PARAMETER | SYMBOL | VALUE | UNIT | NOTE |
|---|---|---|---|---|
| channels | chNo | 4 | | |
| Data Rate | DR | 1… 29 | Gbps | 1) |
| Data Format | | NRZ | | |
| PRBS Pattern | | 9, 15, 31 | | |
| Differential Data Output Amplitude | $D_{OutP/N}$ | 200…800 | $mV_{pp}$ | setting range, 3) |
| Output Jitter (RMS) | $J_{rms}$ | 200 | fs | Typical, 2) |
| Single ended Data Output Impedance | $Z_{Ose}$ | 50 | Ω | Typical |
| Data Output Termination | | AC - coupled | | |
| Clock Input / Output Frequency | $F_{Clk}$ | 0.5…14.5 | GHz | |
| Clock Input / Output Termination | | AC - coupled | | |

**Note:**

1) Output of clock signal is used for daisy chaining additional modules. Maximum daisy chain length is four.
2) RJ measured with CLK pattern. Depends on applied clock signal (measured with CLK20-2 Module, RJ=200fs)
3) Measured at 1GBd at the static High/ Low level of the signal with de-emphasis=0dB.
The eye height at higher data rates might differ.




SYSTEM SOLUTION
clock source, pattern generator, error detector

ELECTRICAL EYE-DIAGRAM
PRBS9, Data Rate = 25 Gbps

## XBERT PLATFORM: LETS YOU START SMALL AND GROW

*PARALLEX*® is a low-cost, modular Bit Error Rate Test Platform used for verification and test of up to 29 Gbps optical and electrical chips, sub-assemblies and system designs. *PARALLEX*® allows users to perform several BER tests at once using a single clock source. The system is ideal for developers desiring to run simultaneous BER tests on parallel interfaces or multiple independent interfaces. *PARALLEX*® is scalable so users can start off with a single channel and add modules to grow the system. Manufacturers can realize great savings by taking advantage of the *PARALLEX*® system's scalability to perform parallel testing in volume production environments.

EUROPÄISCHE UNION
Europäischer Fonds für regionale Entwicklung
Investition in Ihre Zukunft

Am Borsigturm 13
13507 Berlin-Germany
+49 30 814 512 40 00 ph
+49 30 814 512 40 20 fax
www.luceotec.com
sales@luceotec.com

LUCEO TECHNOLOGIES

EPG428

Product Brief