Pattern Generator Module

L-6001-EPG428-1

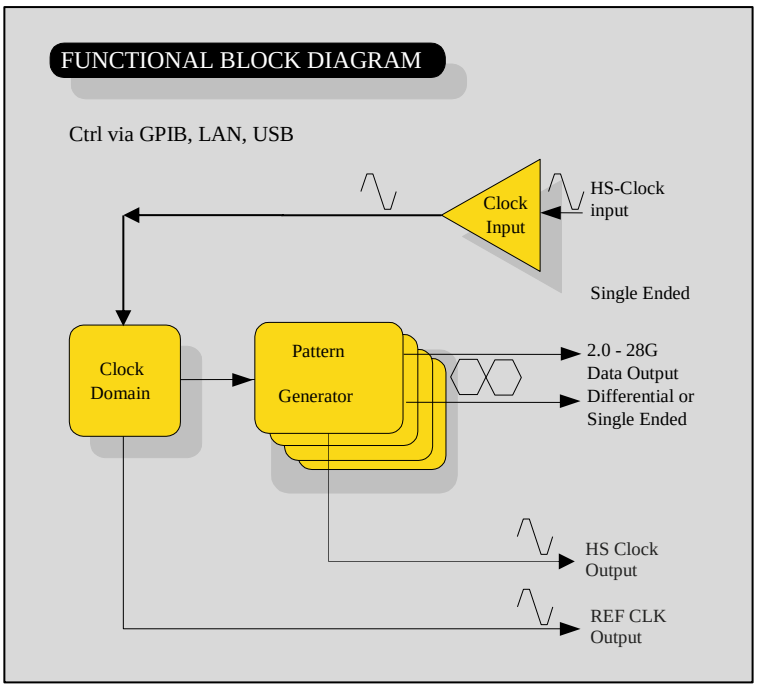
DESCRIPTION

EPG428 is an Electrical Pattern Generator module that plugs into the *ParalleX*® Chassis. EPG428 can generate 4 channel electrical data from 2 Gb/s up to 28 Gb/s. Clock operates with a half rate and can be daisy-chained.
Therefore it is an ideal solution for 100Gb/s and future 400Gb/s applications.

PATTERN GENERATOR MODULE PN: L-6001-EP428-1

KEY FEATURES

- Data Rates 2.0 to 28.2 Gbps
- 4 channels
- Operates with half rate clock
- Differential Electrical Pattern Generator (K Connector)
- Reference clock output to drive SERDES, CDR that require low speed clock
- PRBS pattern: 9, 15, 31
- Data output polarity swap
- High speed Clock Input and Output
- GPIB/LAN/USB Interface via PARALLEX® Chassis.
- Small size: width 50.8mm (2”)



EPG428

Product Brief

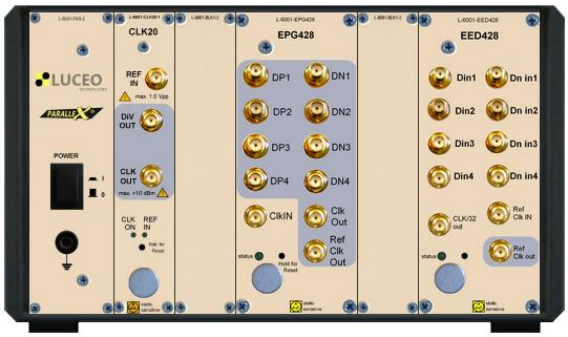
Pattern Generator Module L-6001-EPG428-1

KEY PERFORMANCE PARAMETERS

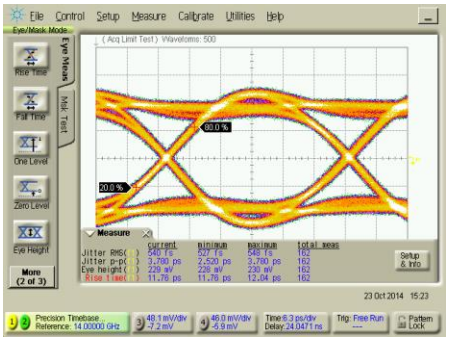
PARAMETER	SYMBOL	Min	Max	UNIT	NOTE
channels	chNo		4		
Data Rate	DR	2.0	28.2	Gbps	1)
Data Formats			NRZ		
PRBS Pattern			9, 15, 31		
Differential Data Output Amplitude	$D_{OutP/N}$	200	800	mV_{pp}	setting range, 3)
Output Jitter (RMS)	J_{rms}		850	fs	2)
Total Jitter (TJ)	TJ		7	ps	
Single ended Data Output Impedance	Z_{Ose}	45	55	Ω	
Data Output Termination			AC - coupled		
Clock Input / Output Frequency	F_{Clk}	1.0	14.1	GHz	
Clock Input / Output Termination			AC - coupled		

Note:

1) Output of clock signal is used for daisy chaining additional modules. Maximum daisy chain length is four.
2) RJ measured with CLK pattern. Depends on applied clock signal (measured with CLK20-2 Module, RJ=200fs)
3) Measured at 1GBd at the static High/ Low level of the signal with de-emphasis=0dB.
The eye height at higher data rates might differ.



SYSTEM SOLUTION
clock source, pattern generator, error detector



ELECTRICAL EYE-DIAGRAM
PRBS31, Data Rate = 28 Gbps

XBERT PLATFORM: LETS YOU START SMALL AND GROW

ParalleX® is a low-cost, modular Bit Error Rate Test Platform used for verification and test of up to 28 Gbps optical and electrical chips, sub assemblies and system designs. *ParalleX*® allows users to perform several BER tests at once using a single clock source. The system is ideal for developers desiring to run simultaneous BER tests on parallel interfaces or multiple independent interfaces. *ParalleX*® is scalable so users can start off with a single channel and add modules to grow the system. Manufacturers can realize great savings by taking advantage of the *ParalleX*® system's scalability to perform parallel testing in volume production environments.

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