Error Detector Module

L-6001-EED428-2

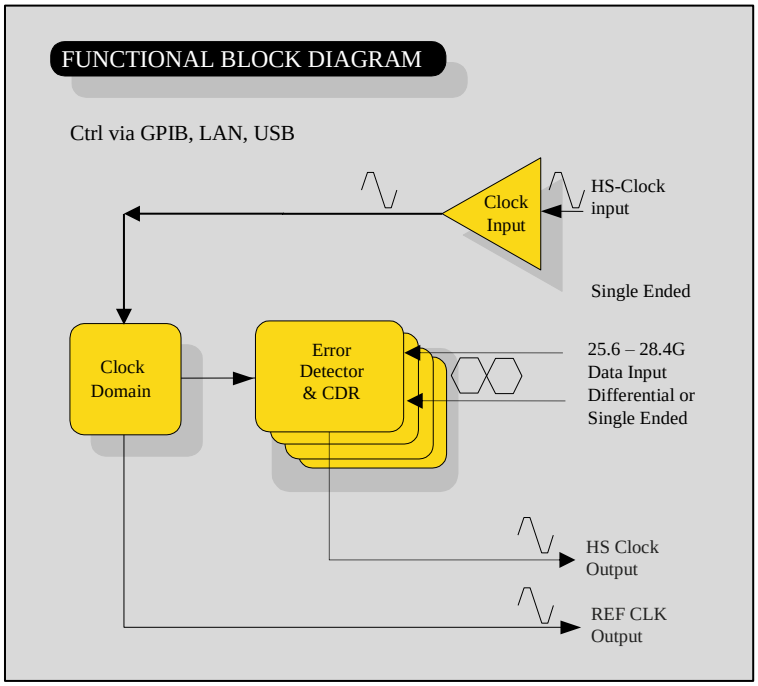
DESCRIPTION

EED428 is an Electrical Error Detector module that plugs into the *PARALLEX*® Chassis. EED428 can check 4 channels electrical data from 22.0 - 28.2Gbps and 8.5Gb/s – 14.1Gb/s . A half-rate input clock is required and it can be daisy-chained to the Pattern Generator and additional modules. Therefore it is an ideal solution for 100Gb/s and future 400Gb/s applications.

ERROR DETECTOR MODULE PN: L-6001-EED428

KEY FEATURES

- Data Rates 22.0 - 28.2Gbps and 8.5Gb/s – 14.1Gb/s Gbps
- 4 channels
- Integrated individual CDR on each channel to track incoming data
- Operates with half rate clock
- Differential Electrical Error Detector (K Connector)
- Reference clock output to drive SERDES, CDR that require low speed clock
- PRBS pattern: 7, 9, 15, 23, 31
- Data input polarity swap
- BER detection down to 1E-15
- High speed Clock Input and Output
- GPIB/LAN/USB Interface via mainframe
- Small size: width 50.8mm (2”)



EED428

Product Brief

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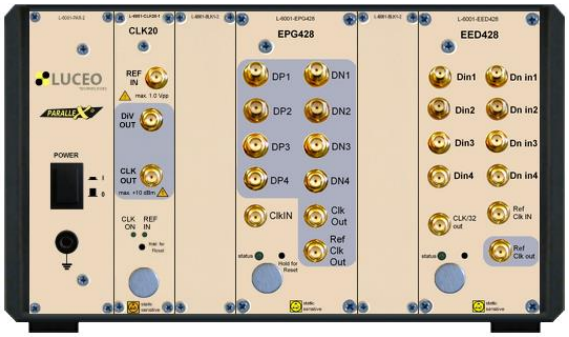
KEY PERFORMANCE PARAMETERS

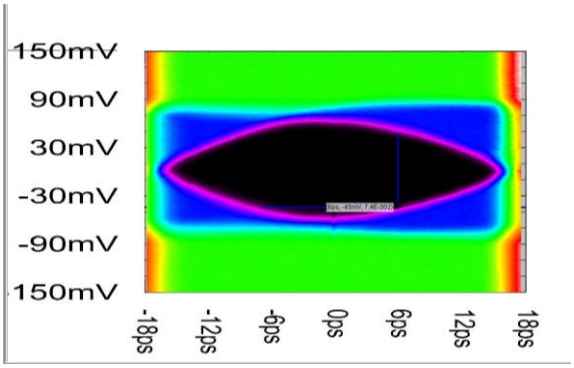
PARAMETER	SYMBOL	Min	Max	UNIT	NOTE
Channels	chNo		4		
Data Rate	DR	8.5 22.0	14.1 28.2	Gbps	1)
Data Formats			NRZ		
PRBS Pattern			7, 9, 15, 23, 31		
Differential Data Input Amplitude	$D_{OutP/N}$	200	1200	mV_{pp}	3), 4)
Differential Data Input Impedance	Z_{Ose}	90	110	Ω	
Data Input Termination			AC - coupled		
Clock Input / Output Frequency	F_{Clk}	12.8	14.2	GHz	2)
Clock Input / Output Termination			AC - coupled		

Note:

1) Apply full rate clock for low data rate range and half rate clock for high data rate range.
2) Additional DR/40 CLK output installed
3) BER of better than 1E-12 can only be achieved if at least the min. input voltage level is applied
4) Minimum input voltage to guarantee error free detection (BER < 10-12) at PRBS31. The input sensitivity of the module will be better for input signals with lower bandwidth, e.g. PRBS7.



SYSTEM SOLUTION
clock source, pattern generator, error detector



Eye scan
Each channel can perform eye scan and bathtub curve

XBERT PLATFORM: LETS YOU START SMALL AND GROW

PARALLEX® is a low-cost, modular Bit Error Rate Test Platform used for verification and test of up to 28 Gbps optical and electrical chips, sub-assemblies and system designs. *PARALLEX*® allows users to perform several BER tests at once using a single clock source. The system is ideal for developers desiring to run simultaneous BER tests on parallel interfaces or multiple independent interfaces. *PARALLEX*® is scalable so users can start off with a single channel and add modules to grow the system. Manufacturers can realize great savings by taking advantage of the *PARALLEX*® system's scalability to perform parallel testing in volume production environments.

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