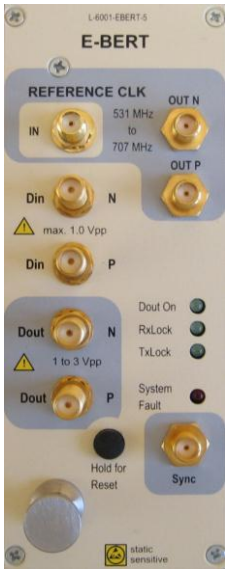
Electrical BERT Module
PN L-6001-EBERT-5

DESCRIPTION

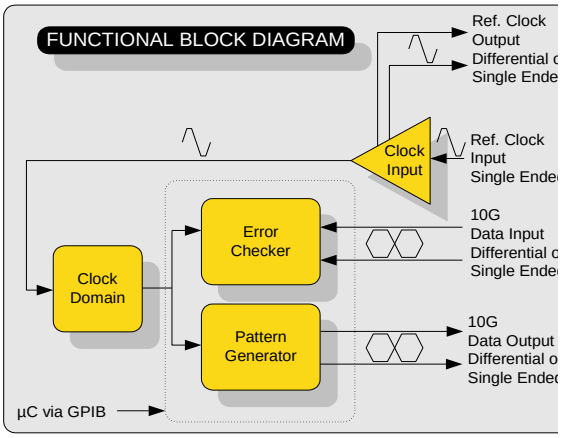
EBERT is a Bit Error Rate Test module that plugs in to the *XBERT* and *ParalleX*™ Chassis. EBERT-5 can generate and receive electrical data from 8.5 Gb/s up to 11.3 Gb/s (options are available to extend this range). User programmable PRBS patterns can be changed via an easy to use GUI. A pattern trigger output provides an electrical trigger synchronous with the pattern for use with an oscilloscope or other test equipment. Front panel indicators give immediate status for Tx and Rx Data.



ELECTRICAL BERT MODULE PN L-6001-EBERT-5

KEY FEATURES

- Data Rates 8.5 to 11.3 Gbps
- Differential Electrical Pattern Generator (SMA Connector)
- Differential Electrical Error Detector (SMA Connector)
- Output crossing adjustable from 20% to 80%
- Variable data output level from 1 to 3V
- PRBS: 7, 9, 10, 11, 15, 21, 23, 31
  User-Pattern: 8Bit - 8Kbyte
  Clock-Pattern: $^1/_1$, $^1/_2$, $^1/_4$, $^1/_8$
  Additional: K28.0-K28.7, CJPAT, SSPS-64 and others
- Data output polarity swap and Data input polarity swap
- BER detection: 0.5 to < 10E-15
- Single error and error rate injection:1 E-3 to 1E-15
- Data log Gating-time: up to 5000h
- Reference Clock Input (single ended) and Output (diff)
- GPIB/LAN/USB Interface via XBERT Chassis.
- Small size: width 50.8mm (2”)



XBERT PLATFORM: LETS YOU START SMALL AND GROW

XBERT is a low-cost, modular Bit Error Rate Test Platform used for verification and test of 10Gb/s and above optical and electrical chip, sub assembly and system designs. *Parallex*® allows users to perform several BER tests at once using a single clock source. The system is ideal for developers desiring to run simultaneous BER tests on parallel interfaces or multiple independent interfaces. *XBERT* and *Parallex*® are scalable so users can start off with a single channel and add modules to grow the system. Manufacturers can realize great savings by taking advantage of the *XBERT* and *Parallex*® system’s scalability to perform parallel testing in volume production environments.

EBERT5 Module Product Overview

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KEY PERFORMANCE PARAMETERS

PARAMETER	SYMBOL	Min	Max	UNIT	NOTE
Data Rate	DR	8.5 (8.0)	11.3	Gbps	
Data Formats			NRZ		
PRBS Pattern			7, 9, 10, 11, 15, 21, 23, 31		
User-Defined Pattern		8	65536	Bit	Note 4
Data Output Signal Channel P or N (single ended)	$D_{OutP/N}$	1	3	V_{pp}	Others available on request
Data Output Rise and Fall time	t_r / t_f	Typical	23	ps	20% - 80%
Output Jitter	J_{rms}	Typical	1.5	ps	Note 5
Crossing	Cr	20	80	%	Adjustable
Differential Output Impedance	Z_{ODiff}	90	110	Ω	
Data Output Termination		AC - coupled			
Measurable Bit Error Rate	BER	<10E-15	0.5		Note 1
Data Input Signal Channel P or N	$D_{InP/N}$	100	1000	mV_{pp}	Single ended
Differential Data Input signal (D_{InDiff}=D_{InP}-D_{InN})	D_{InDiff}	200	2000	mV_{pp}	Note 2
Differential Input Impedance	Z_{InDiff}	90	110	Ω	
Data Input Termination		AC - coupled			
Reference Clock Input Frequency	P_{ref}	531.25	707.35	MHz	
Reference Clock Input Impedance	Z_{Ref}	45	55	Ω	
Reference Clock Input Termination		AC - coupled			
Sync Signal	Sync	550	1100	mV_{pp}	Note 3
Operating Temperature	T_{OP}	0	40	°C	Ambient temp.

Note:

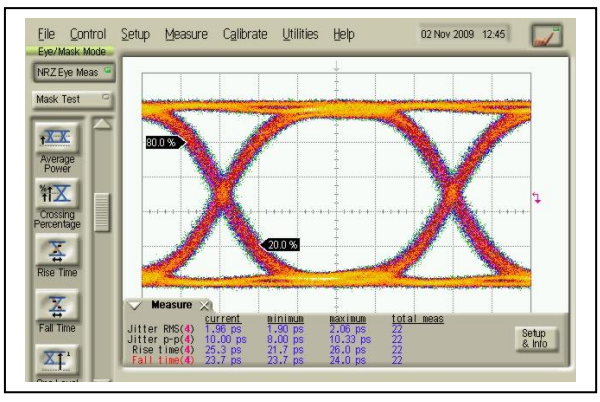
1 BER of better than 10E-15 can only be achieved if the min input voltage level is applied

2 Minimum input voltage to guarantee error free detection (BER < 10^{-15})

3 Default function is pattern trigger. Other functions like pulse per error byte are possible. For more detailed information contact Luceo Technologies

4 Pattern input from 8 to 128 bit in 8 bit steps and from 128 to 65536 bit in 128 bit steps. Preset patterns eg K28.5, CJPAT etc are available on request

5 Measured at: duty cycle 50%, PRBS31, DR= 11.3Gbps, output voltage= 2V, BER= 1E-12



ELECTRICAL EYE-DIAGRAM Duty cycle 50%, PRBS31, DR=11.3Gbps, output voltage=2.5V

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